ABSTRACT OF THE DISCLOSURE

Each chip includes, in addition to a core logic, a register such as a BSR. A TAPC for controlling the register is provided only on a chip of the first stage, and an test commands/data output and input signal lines for the boundary scan test are connected to each other via wire to form a loop. Other signal lines used in the test are distributed from an output signal line of the chip of the first stage. As a result, the test needs to be carried out only once with a smaller number of pins and the number of steps and area can be reduced in chips not provided with TAPC. With this arrangement, in a stacked device in which a plurality of chips are integrally sealed, the boundary scan test only needs to be carried out once with a smaller number of pins.